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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,010	01/07/2004	Toshimichi Seike	OKI.353D	4662

20987 7590 10/04/2005

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/752,010	SEIKE, TOSHIMICHI	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11 and 15-18* is/are rejected.

7)☒ Claim(s) *12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 11, 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bechade et al (5,430,387).

Bechade shows:

11. An output buffer circuit (Fig. 2) comprising:

an input terminal (124) for receiving an input signal;

an output terminal (188) for outputting an output signal;

a first inverter (110 & 106) connected to the input terminal, the first inverter outputting (all circuit required time to rise up and fall down) a first signal having a slow rise up and fall down characteristic;

a second inverter (128 & 130) connected to the input terminal, the second inverter outputting a second signal having the slow rise up and fall down characteristic (all circuit required time to rise up and fall down);

a pull up control circuit (158, 146, 140) connected to the input terminal, the pull up control circuit pulling up a voltage of the first signal during a predetermined time (delay signal) from a time when the input signal is changed from "L" level to "H" level;

a pull down control circuit (182, 170, 166) connected to the input terminal, the pull down control circuit pulling down a voltage of the second signal during a predetermined time (delay signal) from a time when the input signal is changed from "H" level to "L" level;

a first output transistor (102) having a source connected to a first power source potential node (103), a drain connected to the output terminal and a gate connected to the first inverter so as to receive the first signal; and

a second output transistor (104) having a source connected to a second power source potential node (ground), a drain connected to the output terminal and a gate connected to the second inverter so as to receive the second signal.

15. An output buffer circuit according to claim 11, wherein the pull up control circuit includes,

a delay circuit (158 & 146) having an input terminal (114) connected to the input terminal of the output buffer circuit and having an output terminal (142), and a pull up transistor (140) having a first terminal connected to the first power source potential node (141), a second terminal connected to an inverter output terminal of the first inverter and a gate (144) connected to the output terminal of the delay circuit.

16. An output buffer circuit according to claim 11 , wherein the pull down control circuit includes,

a delay circuit (182 & 170) having an input terminal connected to the input terminal of the output buffer circuit and having an output terminal, and a pull down transistor (166) having a first terminal connected to the second power source potential

node (ground), a second terminal connected to an inverter output terminal of the second inverter and a gate (167) connected to the output terminal of the delay circuit.

17. An output buffer circuit according to claim 11, further comprising an enable gate circuit (112 & 134) having a first input terminal (116) connected to the input terminal of the output buffer circuit, a second input terminal (126) connected to receive an enable signal and a pair of output terminals (114 & 136) respectively connected to inverter input terminals of the first and second inverters.

Claim Rejections - 35 USC § 103

3. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bechade et al (5,430,387) in view of Popat et al (5,804,990).

Bechade discloses the claimed invention except that an AND circuit and an OR circuit instead of a NOR gate and a NAND gate. Popat discloses that the AND circuit and the OR circuit is an equivalent structure known in the art (col. 1, line 63 to col. 2, line 3). Therefore, because these two logic gate were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute an AND circuit and an OR circuit for a NOR gate and a NAND gate.

Allowable Subject Matter

4. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

9/29/05